WITH FOUNDRY OFFER AND GROWING ECOSYSTEM, SOI GAINS MOMENTUM AS A FIRM FAVORITE FOR CONSUMER AND IoT APPLICATIONS

Latest Technology Workshop on FD-SOI and RF-SOI Coming to San Francisco This Week

San Francisco, CA, February 26, 2015 – The SOI Industry Consortium announces silicon-on-insulator (SOI) technologies gaining strong industry momentum towards a rapidly growing SOI ecosystem with a robust foundry offer and leading fabless players demonstrating how simple it is today to design and manufacture integrated circuits on fully depleted SOI (FD-SOI) and radio-frequency SOI (RF-SOI) technologies, confirming SOI as a very competitive technology platform for fast-growing semiconductor applications.

Recent workshops organized by the consortium in Shanghai, China and Tokyo, Japan have highlighted market momentum for SOI with technical contributions presented by leading integrated device manufacturers (IDM), fabless semiconductor companies, foundries, EDA vendors and circuit designers, and all members of the global SOI ecosystem, stimulating discussions and sharing information about competitive benchmarks, end-product results, technology milestones and emerging applications. As evidence, the consortium points to the solution-oriented technical papers and growing international participation at SOI workshops, including the upcoming SOI-organized event in San Francisco tomorrow, February 27th.

“It is important to stress that the SOI technologies, in particular FD-SOI and RF-SOI, are best positioned to address the next big inflexion point of the IC community known as the Internet of Things (IoT),” commented Carlos Mazure, Executive Director of the SOI Consortium. “The SOI product and technology platforms combine lowest power consumption and strong performance at low voltage supply while remaining very cost competitive.”

The developing IoT wave will change the way the IC industry has approached IC development by enabling optimized “low power-performance and reduced-area” solutions for better battery lifetime and increased functionality.

The workshop is organized by Dr. Mendez, Dr. Olivier Faynot, head of CMOS technology at CEA-Leti, and Dr. Carlos Mazure, chief technology officer of Soitec.

Registration is free by registering at :http://www.soiconsortium.org/workshops/sanfrancisco/

About the SOI Industry Consortium

The SOI Industry Consortium is chartered with accelerating silicon-on-insulator (SOI) innovation into broad markets by promoting the benefits of SOI technology and reducing the barriers to adoption. Representing innovation leaders from the entire electronics industry infrastructure, current SOI Industry Consortium members include: AMD, Altera Corp., ARM, Cadence Design Systems, CEA-Léti, FEI, GLOBALFOUNDRIES, IBM, IMEC, Infotech, Kanazawa Institute of Technology, KLA-Tencor, MEMC, Mentor Graphics, MIT Lincoln Laboratories, Nvidia, Ritsumeikan University, Samsung, Semico, SEH Europe, Soitec, Stanford University, STMicroelectronics, Synopsys, Tyndall Institute, University of California-Berkeley, University Catholique de Louvain and UMC. Membership is open to all companies and institutions throughout the electronics industry.

For more information, please visit www.soiconsortium.org

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