



PRESS RELEASE

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“Places2Be” project to boost European leadership around FD-SOI – the faster, cooler, simpler chip technology

- 3-year, €360M project involves 19 partners across Europe, led by STMicroelectronics
- 2 FD-SOI manufacturing pilot lines to be located in Grenoble and Dresden
- Places2Be is supported by the ENIAC JU and the National Public Authorities

Brussels, May 21 2013 – The launch of *Places2Be*, a 3-year, €360M advanced-technology pilot-line project to support the industrialization of *Fully-Depleted Silicon-On-Insulator (FD-SOI)* microelectronics technology was announced today by a group of 19 leading European companies and academic institutions.

Led by STMicroelectronics (NYSE: STM), a global semiconductor leader serving customers across the spectrum of electronics applications, *Places2Be* (“*Pilot Lines for Advanced CMOS Enhanced by SOI in 2x nodes, Built in Europe*”) aims to support the deployment of a FD-SOI pilot line at 28nm and the subsequent node, as well as a dual source that will enable volume manufacturing in Europe. *Places2Be* will drive the creation of a European microelectronics design ecosystem using this FD-SOI platform and explore the path towards the next step for this technology (14/10nm).

FD-SOI is a low-power, high-performance next-generation alternative to conventional (“bulk”) silicon and FinFET technologies. The first FD-SOI systems-on-chips are expected to be used in consumer electronics, high-performance computing and networking.

With a budget of nearly €360M, the participation of 19 partners from 7 countries, and the planned involvement of about 500 engineers over three years across Europe, *Places2Be* is the largest ENIAC Joint Undertaking project to date and is supported as well by the National Public Authorities in the participating countries. *Places2Be* is one of the key enabling technologies (KETs) pilot-line projects contracted by the ENIAC JU to develop technologies and application areas with substantial societal impact.

The FD-SOI manufacturing sources for the project are located in each of the two largest European microelectronics clusters: the pilot line in STMicroelectronics’ Crolles fab (near Grenoble, France) and the dual source in GlobalFoundries’ fab 1 in Dresden (Germany).

“*The Places2Be project will reinforce the ecosystems of both Grenoble and Dresden clusters, while also positively impacting the whole value chain of microelectronics in Europe – large companies, SMEs, start-ups and research organizations – beyond the direct impact induced by the material and IP investments,*” declared François Finck, Director of ST’s R&D cooperative programs and project coordinator.



Note to editors

Places2Be members (in alphabetic order)

- ACREO Swedish ICT AB, Sweden
- Adixen Vacuum Products, France
- Axiom IC, Netherlands
- Bruco Integrated Circuits, Netherlands
- Commissariat à l'énergie atomique et aux énergies alternatives, France
- Dolphin Integration, France
- Ericsson AB, Sweden
- eSilicon Romania S.r.l., Romania
- Forschungszentrum Jülich GmbH, Germany
- GlobalFoundries Dresden, Germany
- Grenoble INP, France
- IMEC Interuniversitair Micro-Electronica Centrum vzw, Belgium
- Ion Beam Services, France
- Mentor Graphics France Sarl, France
- SOITEC SA, France
- ST-Ericsson
- STMicroelectronics (Crolles2 SAS, SA, Grenoble SAS), France
- Université Catholique de Louvain, Belgium
- University of Twente, Netherlands

Countries involved:

- Belgium
- Finland
- France
- Germany
- Romania
- Sweden
- The Netherlands

About FD-SOI

FD-SOI stands for “Fully-Depleted Silicon-On-Insulator.” This technology improves the electrostatic control of the transistor channel, improving transistor performance and power efficiency. More precisely Places2Be uses Ultra-Thin Body and Buried oxide (UTBB) FD-SOI, which allows the dynamic tuning of transistor performance, from low power to high speed, during operation. A video introduction to this technology is available on YouTube:

www.youtube.com/watch?v=S_wMzAEajO0&list=UUU5iH94nyLSQAn6SgDM9Iag&index=1



About the ENIAC JU

The ENIAC Joint Undertaking (JU) is a public-private partnership on nanoelectronics bringing together the ENIAC member States, the European Union, and AENEAS (an association representing European R&D actors in this field).

It coordinates research activities through competitive calls for proposals to enhance the further integration and miniaturization of devices, and increase their functionalities. It shall deliver new materials, equipment and processes, new architectures, innovative manufacturing processes, disruptive design methodologies, new packaging and 'systemising' methods. It will drive and be driven by innovative high-tech applications in communication and computing, transport, health care and wellness, energy and environmental management, security and safety, and entertainment.

The ENIAC JU was set up in February 2008 and will allocate grants throughout 2013. The projects selected for funding shall be executed till 31 December 2017. The total value of the R&D activities generated through ENIAC JU is estimated at 3 B€.

About STMicroelectronics

ST is a global leader in the semiconductor market serving customers across the spectrum of sense and power and automotive products and embedded processing solutions. From energy management and savings to trust and data security, from healthcare and wellness to smart consumer devices, in the home, car and office, at work and at play, ST is found everywhere microelectronics make a positive and innovative contribution to people's life. By getting more from technology to get more from life, ST stands for life.augmented.

In 2012, the Company's net revenues were \$8.49 billion. Further information on ST can be found at www.st.com

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